IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method for performing a gather operation on a computer processor comprising:

computing addresses for [one or more] a plurality of data elements of a matrix stored in memory;

retrieving [loading] each of said data elements from memory based on the computed addresses [into separate storage locations]; and

executing a plurality of instructions, each instruction depositing [each] one or more of said data elements contiguously with other data elements in a [single] storage location.

2. (Original) The method as in claim 1 wherein said storage locations are registers.

3. (Original) The method as in claim 1 wherein computing addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

4. (Currently amended) The method as in claim 1 [wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said computer processor] further comprising:

loading each of said data elements from memory into separate storage locations prior to executing said plurality of instructions.

5. (Currently amended) The method as in claim [4] 1 wherein said computer processor executes [multiple DEPOSIT] two or more of said instructions in a single clock cycle.

6. (Original) The method as in claim 1 further comprising:

storing each of said data elements on a mass storage device.

7. (Original) The method as in claim 2 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

8. (Currently amended) A method for performing a scatter operation on a computer processor comprising:

calculating addresses in memory to which a plurality of data elements are to be scattered to form a matrix in memory;

executing a plurality of instructions, each of said instructions extracting [each] one or more of said data elements from a storage location in which said data elements are stored contiguously; and

storing said data elements to said addresses in memory.

9. (Original) The method as in claim 8 wherein said storage location is a register.

10. (Currently Amended) The method as in claim 8 wherein [computing] calculating addresses comprises:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

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11. (Currently amended) The method as in claim 8 wherein [extracting] storing each of said data elements is accomplished via [an EXTRACT] a plurality of STORE instructions executed by said computer processor.

12. (Currently amended) The method as in claim [11] 8 wherein said computer processor executes [multiple EXTRACT] two or more of said instructions in a single clock cycle.

13. (Original) The method as in claim 9 wherein said register is 64-bits wide and said data elements are 16-bits in length.

14. (Currently amended) A computer system comprising:

a memory;

a processor communicatively coupled to the memory; and

a storage device communicatively coupled to the processor and having stored therein a sequence of instructions which, when executed by the processor, causes the processor to at least,

compute addresses for [one or more] a plurality of data elements of a matrix stored in memory;

retrieve [load] each of said data elements from memory based on the computed addresses [into separate storage locations;] and

execute a plurality of instructions, each instruction to deposit [each] one or more of said data elements contiguously with other data elements in a [single] storage location.

15. (Original) The computer system as in claim 14 wherein said storage locations are registers.

16. (Original) The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor computes addresses by:

extracting indices for each of said data elements into separate storage locations; and

adding each of said indices to a base address.

17. (Currently amended) The computer system as in claim 14 [wherein depositing each of said data elements is accomplished via a DEPOSIT instruction executed by said processor] wherein said processor loads each of said data elements from memory into separate storage locations prior to executing said plurality of DEPOSIT instructions.

18. (Currently amended) The computer system as in claim 17 wherein said processor executes [multiple DEPOSIT] two or more of said instructions in a single clock cycle.

19. (Original) The computer system as in claim 14 wherein, responsive to one or more instructions in said sequence, said processor further:

stores each of said data elements on said mass storage device.

20. (Original) The computer system as in claim 15 wherein said registers are 64-bits wide and said data elements are 16-bits in length.

Please add the following new claims:

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21. (New) A method as in claim 1 wherein computing addresses comprises:

executing a series of instructions, each instruction to extract an address index for one of said plurality of data elements.

22. (New) The method as in claim 21 wherein said address indices are extracted from a series of contiguous memory locations

23. (New) The method as in claim 21 wherein computing addresses comprises:

adding each of said address indices to a base address.